REMARKS

Claims 1, 5, 15, and 20 have been amended. No new matter has been added. Claims 29-34 have been withdrawn from consideration in response to a restriction requirement imposed by the Examiner. Thus, claims 1, 5-8, 14-15, 17, and 20-23 are pending in the present application.

In the Office Action, claims 1, 5-8, 14-15, 17, and 20-23 were rejected under the judicially created doctrine of obviousness-type double patenting as being obvious over U.S. Patent No. 6,737,320. In the interest of expediency, Applicants have included herein a terminal disclaimer and respectfully request that the Examiner's rejection of claims 1, 5-8, 14-15, 17, and 20-23 be withdrawn. However, it will be appreciated that the filing of the terminal disclaimer to obviate the Examiner's rejection is not an admission of the propriety of the rejection. *Quad Environmental Technologies Corp. vs. Union Sanitary District,* 946 F.2d 870, 20 USPQ2d 1392 (Fed Cir. 1991). See, *e.g.*, MPEP §804.03.

In the Office Action, claims 1, 5-8, 15 and 20 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Lim (U.S. Patent No. 5,841,161). Claims 14, 17, 21 and 23 were rejected under 35 U.S.C. 103(a) as being obvious over Lim. The Examiner's rejections are respectfully traversed.

With regard to independent claims 1 and 15, Applicants describe and claim, among other things, forming a first dielectric layer on a semiconductor substrate and forming a floating gate above the first dielectric layer. The floating gate is comprised of a first layer doped with a first type of dopant material and a second layer doped with a second type of dopant material that is opposite the first type of dopant material in the first layer. Applicants also describe and claim forming a second dielectric layer above the floating gate, forming a control gate above the

second dielectric layer; and forming a source and a drain in the substrate such that the first layer of the floating gate overlaps the source and the drain.

Lim describes forming a first semiconductor layer 23 having an n-type conductivity overlapping a drain 31 formed in a substrate 21. See Lim, col. 3, ll. 34-43 and Figure 4F. The first conductivity-type semiconductor layer 23 is excluded from a region in which in an erase operation occurs, i.e., a region above a source 30. See Lim, col. 2, ll. 49-52. Lim also describes forming a second semiconductor layer 25 having p-type conductivity overlapping a source 30 formed in the substrate 21. Lim further describes forming a third semiconductor layer 27 having an n-type conductivity on the overall surface of the substrate 21 including the second semiconductor layer 25. Lim, however, does not describe or suggest forming a first layer doped with a first type of dopant material, a second layer doped with a second type of dopant material that is opposite the first type of dopant material in the first layer, and a source and a drain in the substrate such that the first layer of the floating gate overlaps the source. Thus, Applicants respectfully submit the claims 1, 5-8, 15 and 20 are not anticipated by Lim and request that the Examiner's rejections of these claims under 35 U.S.C. 102(b) be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the cited prior art. A finding of obviousness under 35 U.S.C. § 103 requires a determination of the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed subject matter and the prior art, and whether the differences are such that the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made. *Graham v. John Deere Co.*, 148 USPQ 459 (U.S. S.Ct. 1966). To determine whether the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made, one should determine whether the prior art

reference (or references when combined) teach or suggest all the claim limitations. Furthermore, it is necessary for the Examiner to identify the reason why a person of ordinary skill in the art would have combined the prior art references in the manner set forth in the claims.

As discussed above, Lim does not describe or suggest all of the limitations of the invention as claimed in independent claims 1 and 15. Furthermore, Lim teaches away from modifying the prior art to arrive at Applicants' claimed invention, i.e., Lim teaches away from forming the floating gate such that the first layer of the floating gate overlaps the source and the drain. In particular, Lim teaches forming a first conductivity-type semiconductor layer 23 that is excluded from a region in which in an erase operation occurs, i.e., a region above the source 30 and a second conductivity-type semiconductor layer 25 overlapping the region in which the erase operation occurs, i.e., a region above the source 30. Neither the layer 23 nor the layer 25 overlaps both the source and the drain regions 30, 31.

Thus, Applicants respectfully submit that the present invention is not obvious over the cited prior art and, in particular, request that the Examiner's rejections of claims 14, 17, 21, and 23 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned attorney at (713) 934-4050 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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